*Fig. 1*

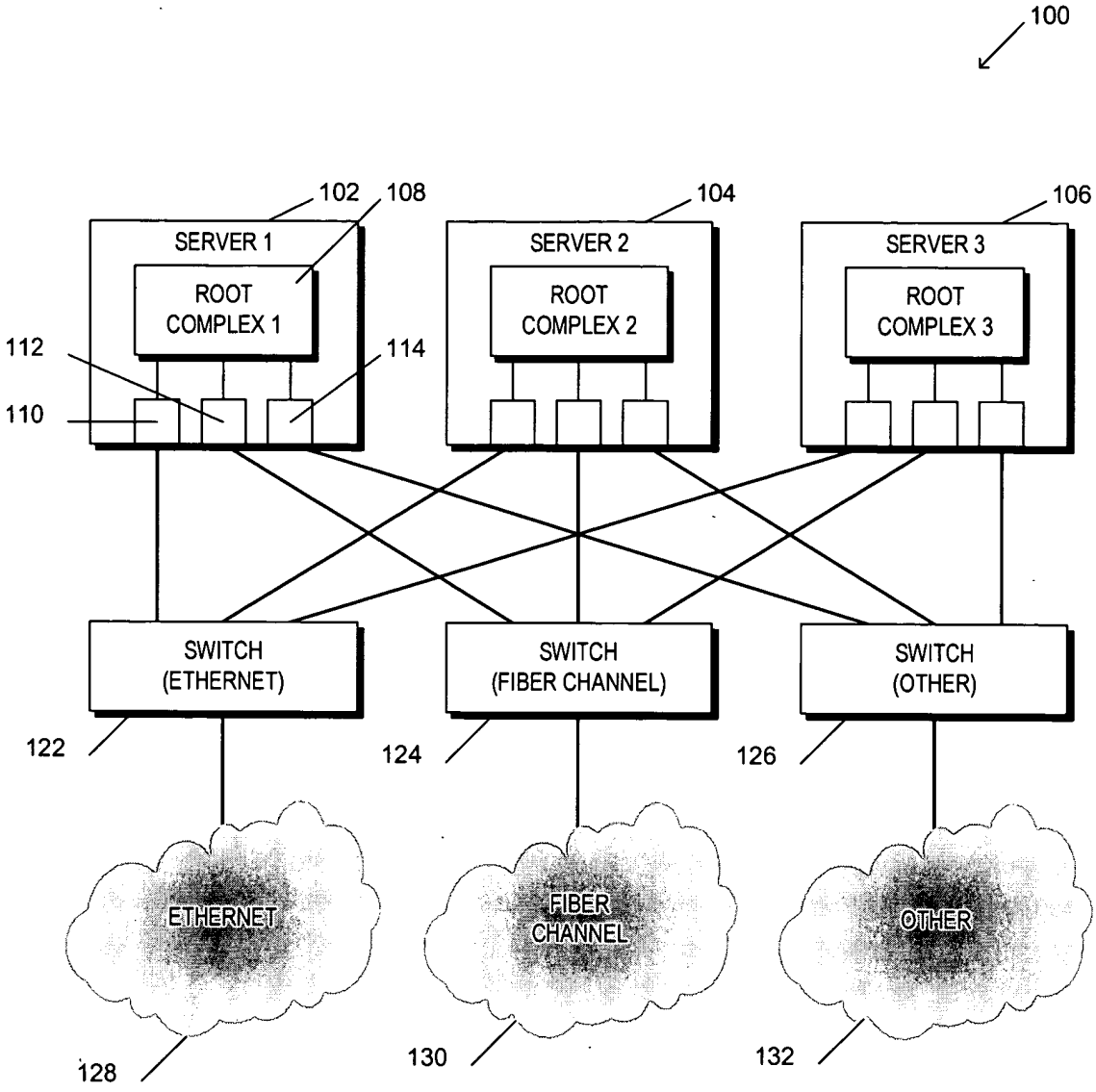

100
102
108
104
106
SERVER 1
ROOT COMPLEX 1
SERVER 2
ROOT COMPLEX 2
SERVER 3
ROOT COMPLEX 3
112
114
110
SWITCH (ETHERNET)
SWITCH (FIBER CHANNEL)
SWITCH (OTHER)
122
124
126
ETHERNET
FIBER CHANNEL
OTHER
128
130
132

Fig. 2A

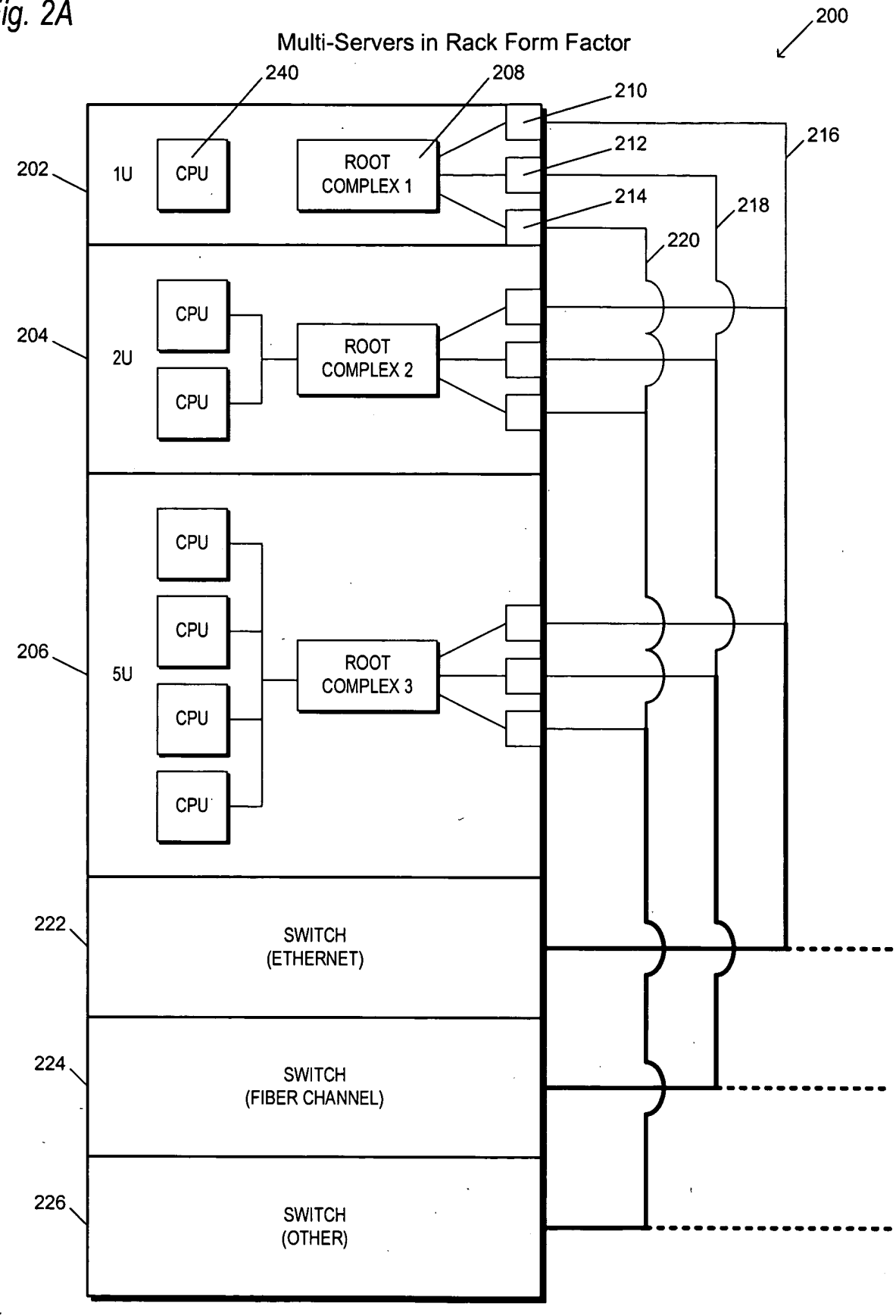

Multi-Servers in Rack Form Factor
200
240
208
210
216
212
214
218
220
202
1U
CPU
ROOT COMPLEX 1
204
2U
CPU
CPU
ROOT COMPLEX 2
206
5U
CPU
CPU
CPU
CPU
ROOT COMPLEX 3
222
SWITCH (ETHERNET)
224
SWITCH (FIBER CHANNEL)
226
SWITCH (OTHER)

*Fig. 2B*

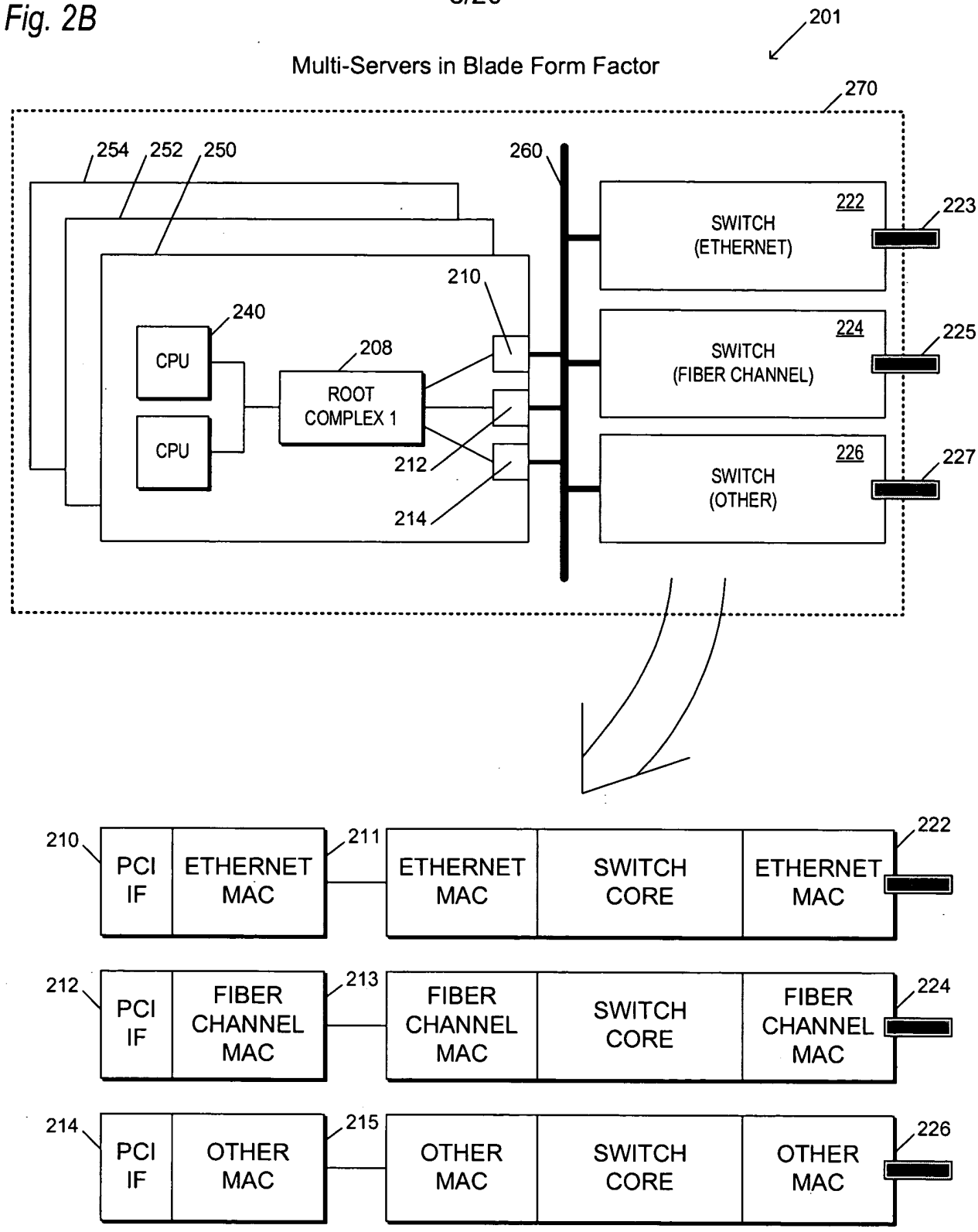

201
Multi-Servers in Blade Form Factor
270
254
252
250
260
222
SWITCH
(ETHERNET)
223
210
240
CPU
208
ROOT
COMPLEX 1
224
SWITCH
(FIBER CHANNEL)
225
CPU
212
226
SWITCH
(OTHER)
227
214
210
PCI
IF
ETHERNET
MAC
211
ETHERNET
MAC
SWITCH
CORE
ETHERNET
MAC
222
212
PCI
IF
FIBER
CHANNEL
MAC
213
FIBER
CHANNEL
MAC
SWITCH
CORE
FIBER
CHANNEL
MAC
224
214
PCI
IF
OTHER
MAC
215
OTHER
MAC
SWITCH
CORE
OTHER
MAC
226

*Fig. 2C*

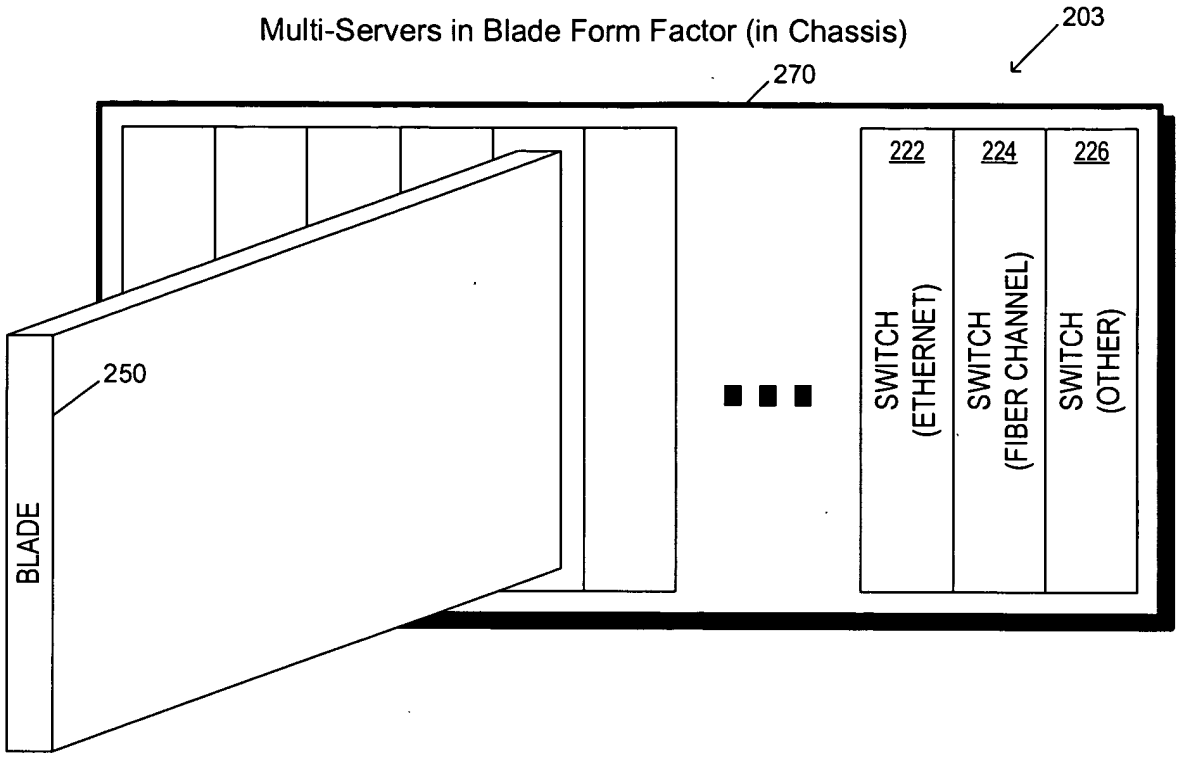

Multi-Servers in Blade Form Factor (in Chassis)
203
270
222
224
226
SWITCH (ETHERNET)
SWITCH (FIBER CHANNEL)
SWITCH (OTHER)
250
BLADE

Fig. 3

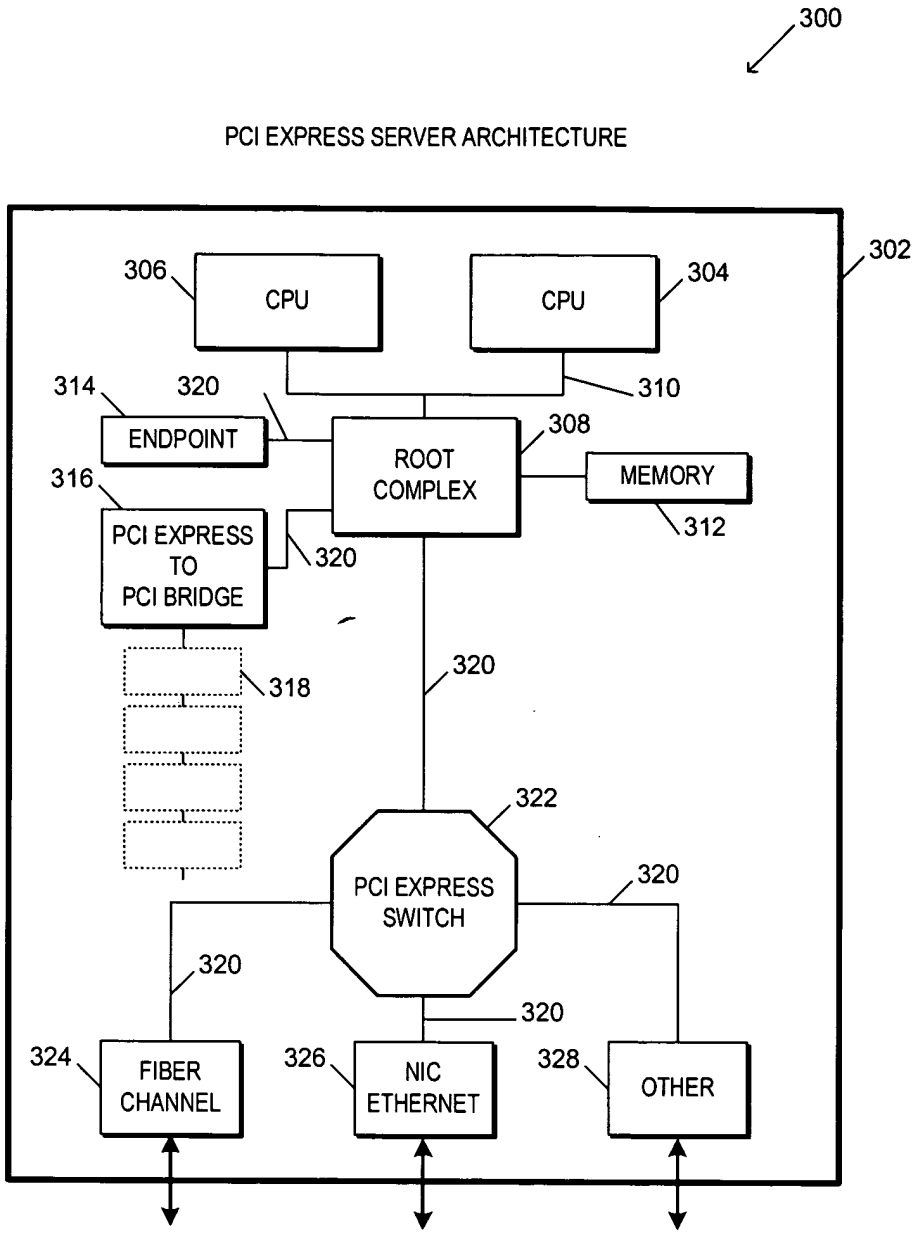

300
PCI EXPRESS SERVER ARCHITECTURE
302
306
CPU
304
CPU
310
314
320
ENDPOINT
308
ROOT COMPLEX
MEMORY
312
316
PCI EXPRESS TO PCI BRIDGE
320
318
320
322
PCI EXPRESS SWITCH
320
320
320
324
FIBER CHANNEL
326
NIC ETHERNET
328
OTHER

Fig. 4

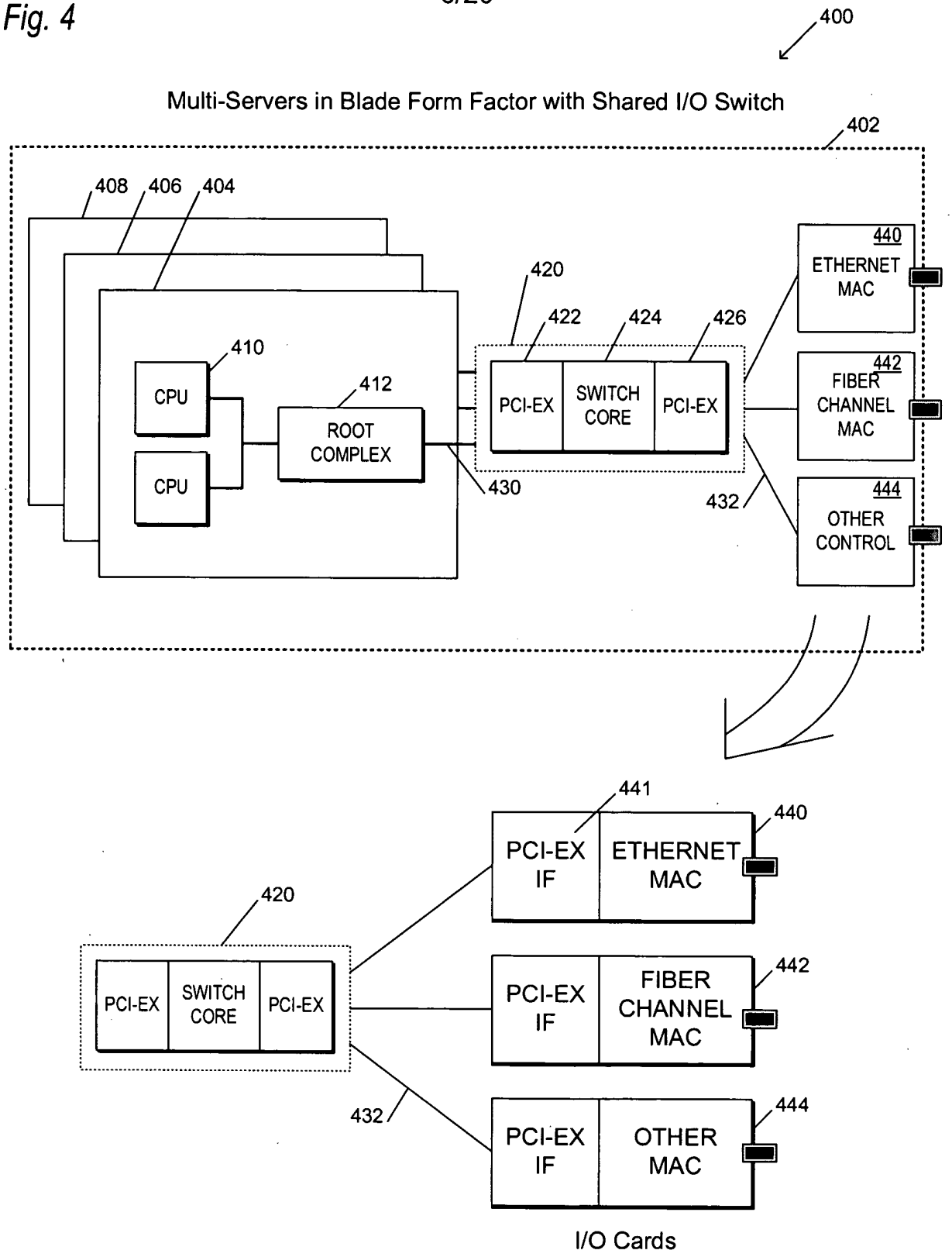

400
Multi-Servers in Blade Form Factor with Shared I/O Switch
402
408
406
404
410
CPU
CPU
412
ROOT COMPLEX
420
422
424
426
PCI-EX
SWITCH CORE
PCI-EX
430
432
440
ETHERNET MAC
442
FIBER CHANNEL MAC
444
OTHER CONTROL
441
PCI-EX IF
ETHERNET MAC
PCI-EX IF
FIBER CHANNEL MAC
PCI-EX IF
OTHER MAC
I/O Cards

Fig. 5

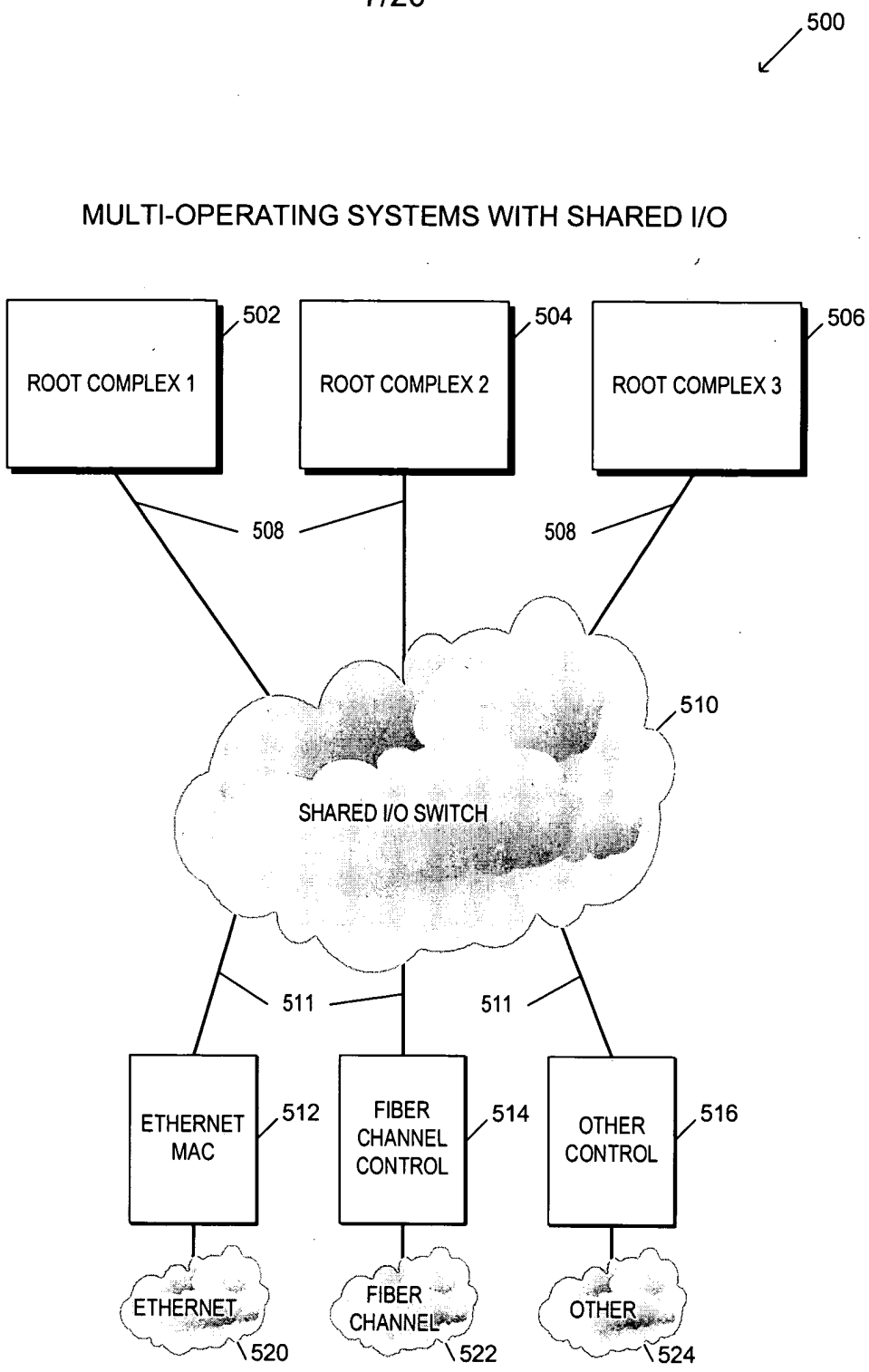

500
MULTI-OPERATING SYSTEMS WITH SHARED I/O
ROOT COMPLEX 1
502
ROOT COMPLEX 2
504
ROOT COMPLEX 3
506
508
508
SHARED I/O SWITCH
510
511
511
ETHERNET MAC
512
FIBER CHANNEL CONTROL
514
OTHER CONTROL
516
ETHERNET
520
FIBER CHANNEL
522
OTHER
524

Fig. 6

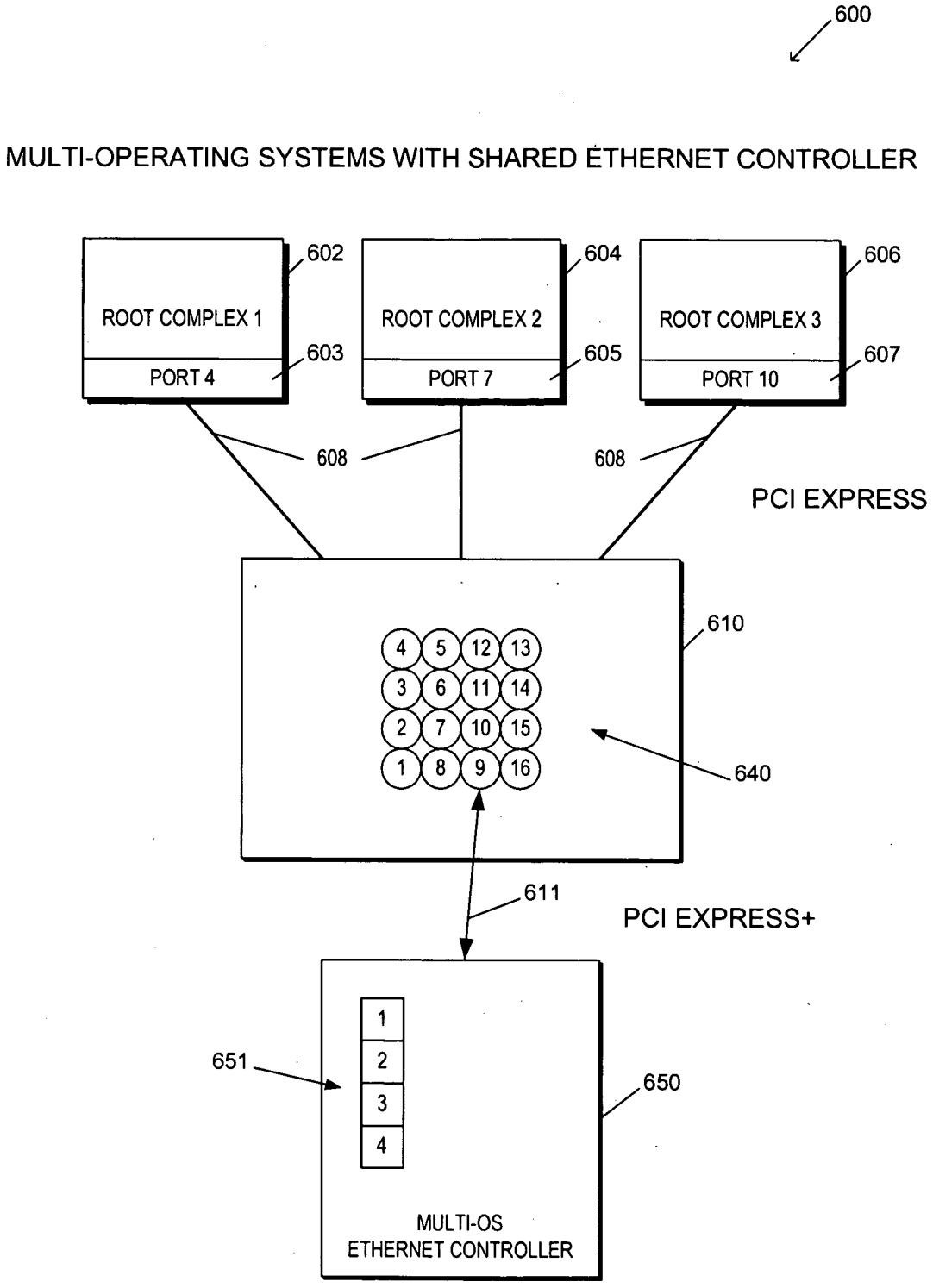

600
MULTI-OPERATING SYSTEMS WITH SHARED ETHERNET CONTROLLER
ROOT COMPLEX 1
602
PORT 4
603
ROOT COMPLEX 2
604
PORT 7
605
ROOT COMPLEX 3
606
PORT 10
607
608
608
PCI EXPRESS
610
4 5 12 13
3 6 11 14
2 7 10 15
1 8 9 16
640
611
PCI EXPRESS+
651
1
2
3
4
650
MULTI-OS
ETHERNET CONTROLLER

Fig. 7

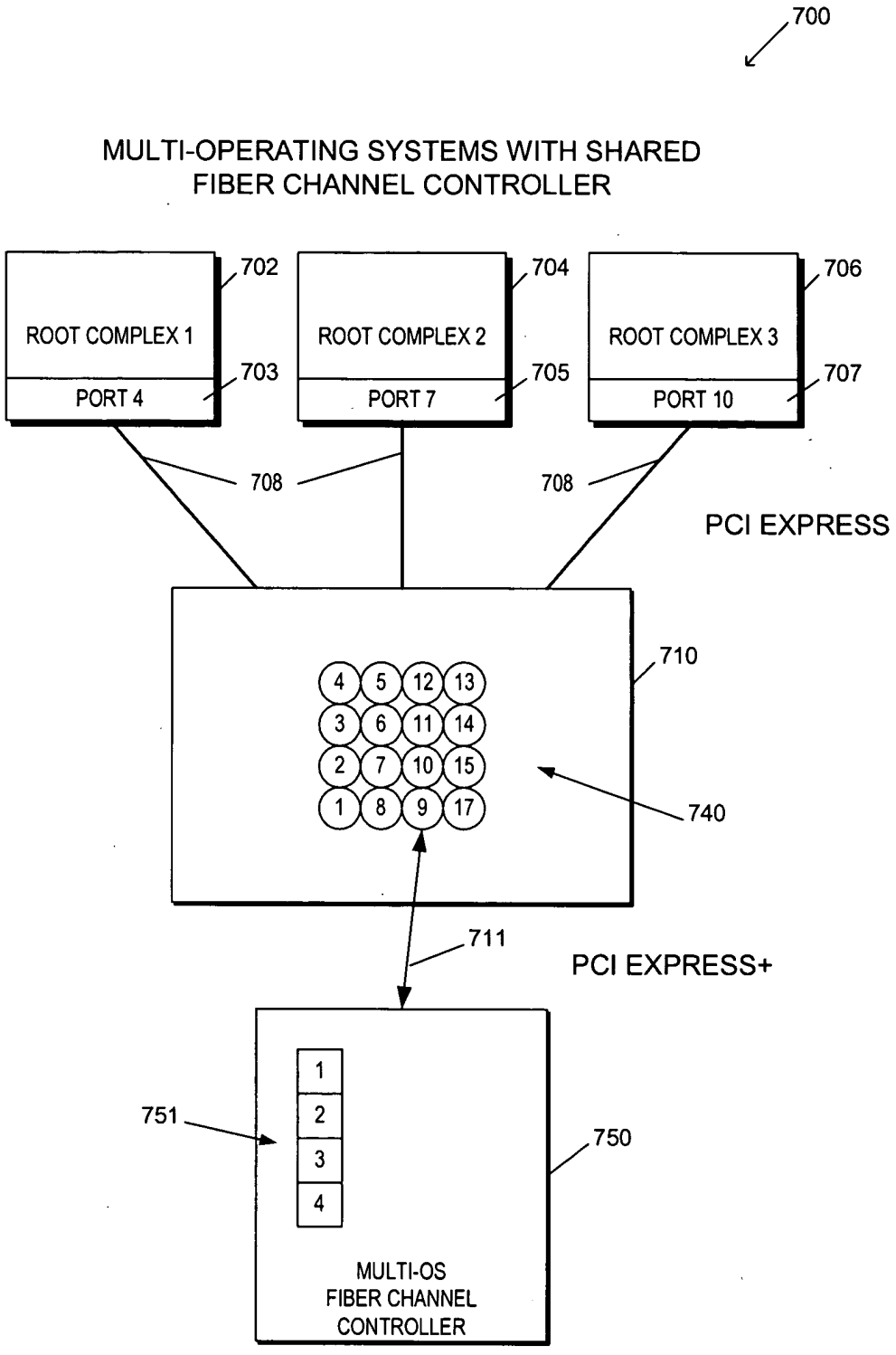

700
MULTI-OPERATING SYSTEMS WITH SHARED FIBER CHANNEL CONTROLLER
ROOT COMPLEX 1
PORT 4
702
703
ROOT COMPLEX 2
PORT 7
704
705
ROOT COMPLEX 3
PORT 10
706
707
708
708
PCI EXPRESS
710
4 5 12 13
3 6 11 14
2 7 10 15
1 8 9 17
740
711
PCI EXPRESS+
751
1
2
3
4
750
MULTI-OS FIBER CHANNEL CONTROLLER

*Fig. 8*

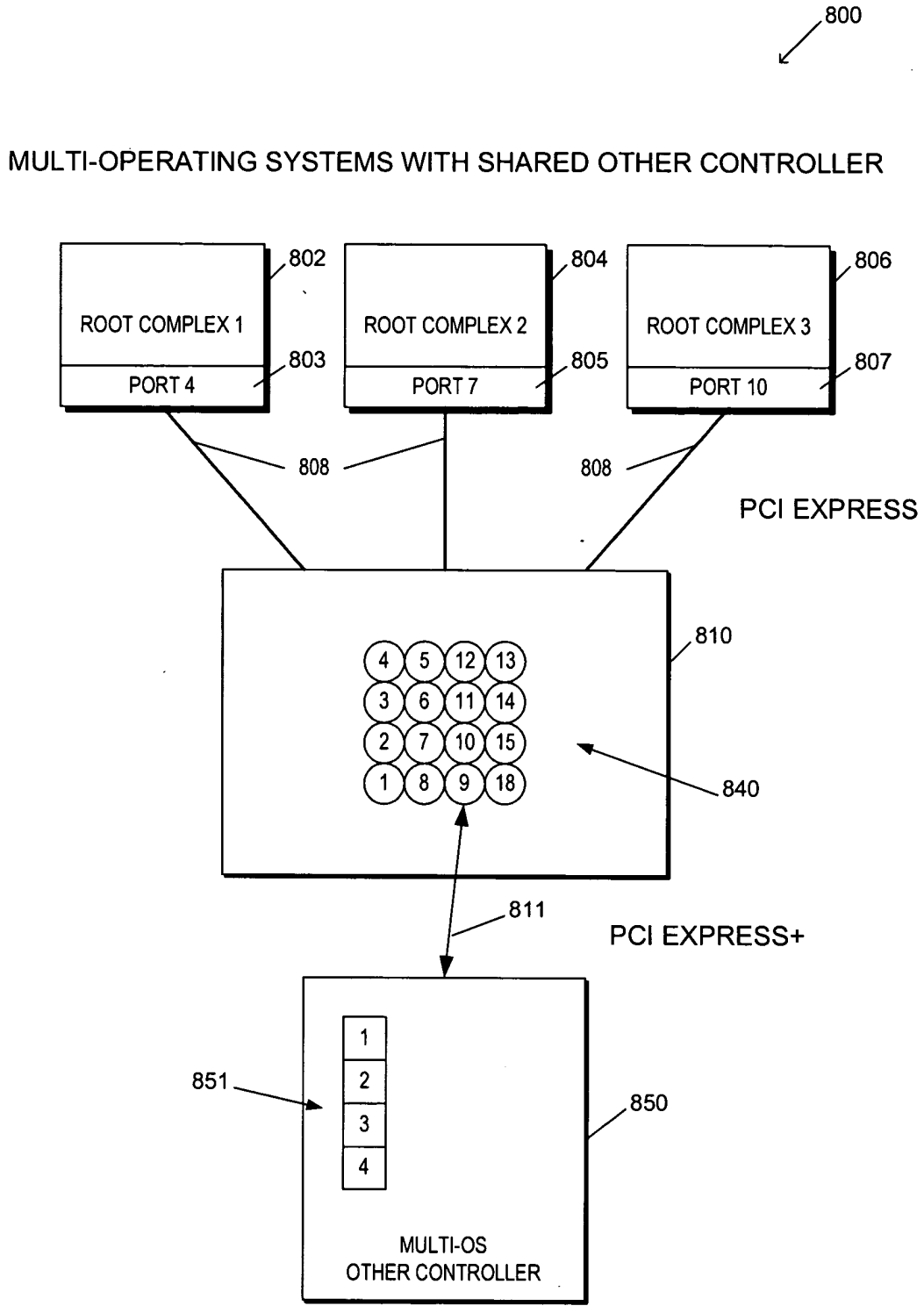

800
MULTI-OPERATING SYSTEMS WITH SHARED OTHER CONTROLLER
ROOT COMPLEX 1
802
PORT 4
803
ROOT COMPLEX 2
804
PORT 7
805
ROOT COMPLEX 3
806
PORT 10
807
808
808
PCI EXPRESS
810
4 5 12 13
3 6 11 14
2 7 10 15
1 8 9 18
840
811
PCI EXPRESS+
851
1
2
3
4
850
MULTI-OS
OTHER CONTROLLER

Fig. 9

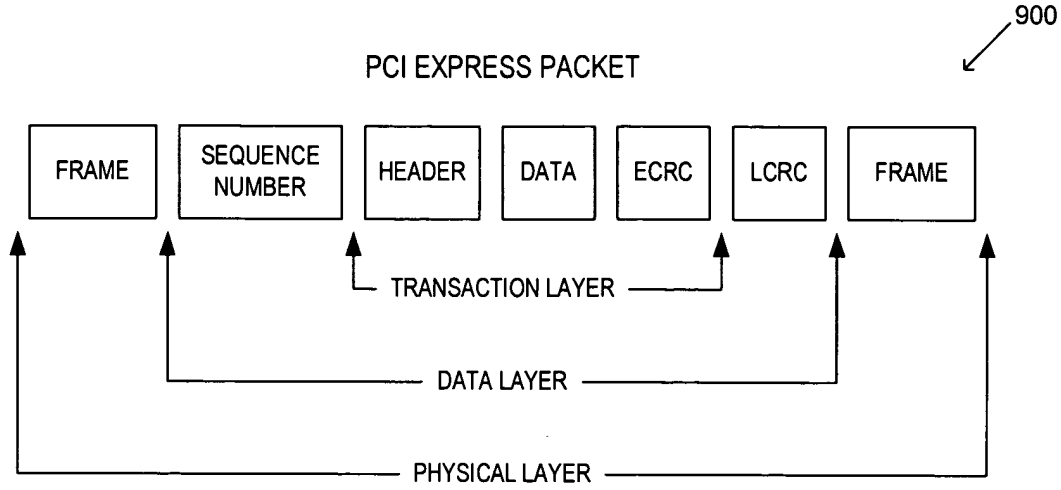



Fig. 10

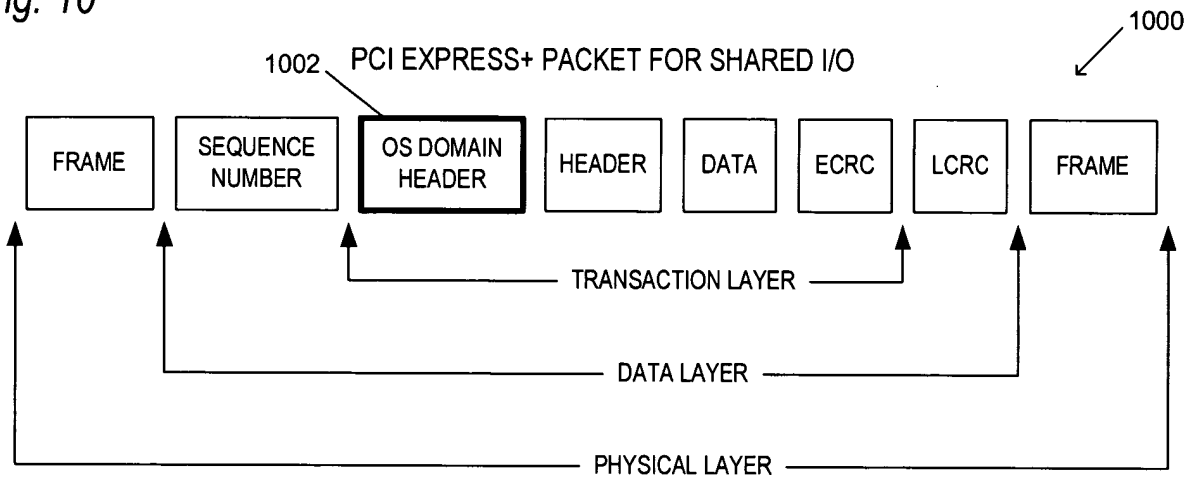
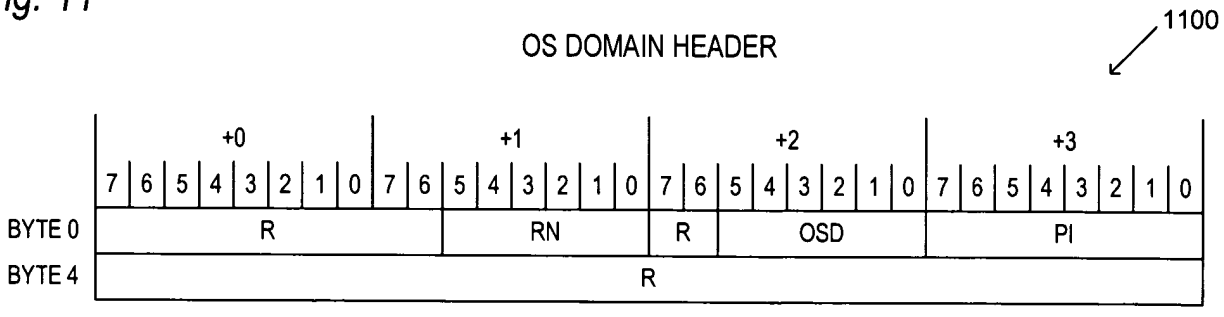



Fig. 11




| | |
|---|---|
| PI | Protocol ID Field |
| OSD | OS Domain Number |
| RN | Resource Number (which buffer the packet belongs to) |
| R | reserved |

*Fig. 12 (Prior art)*

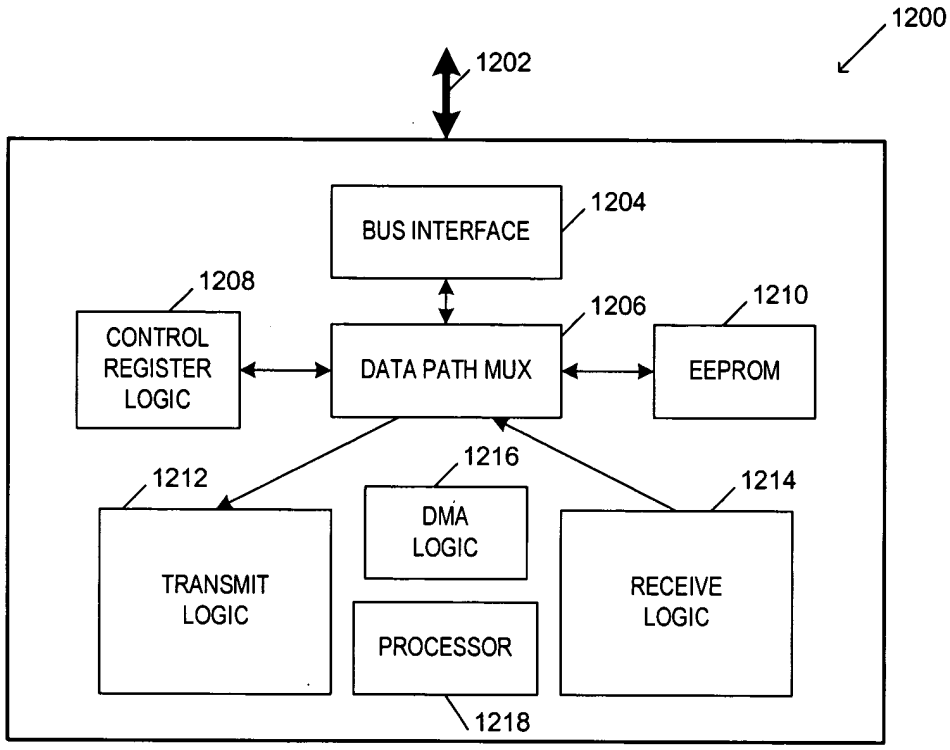


Fig. 13

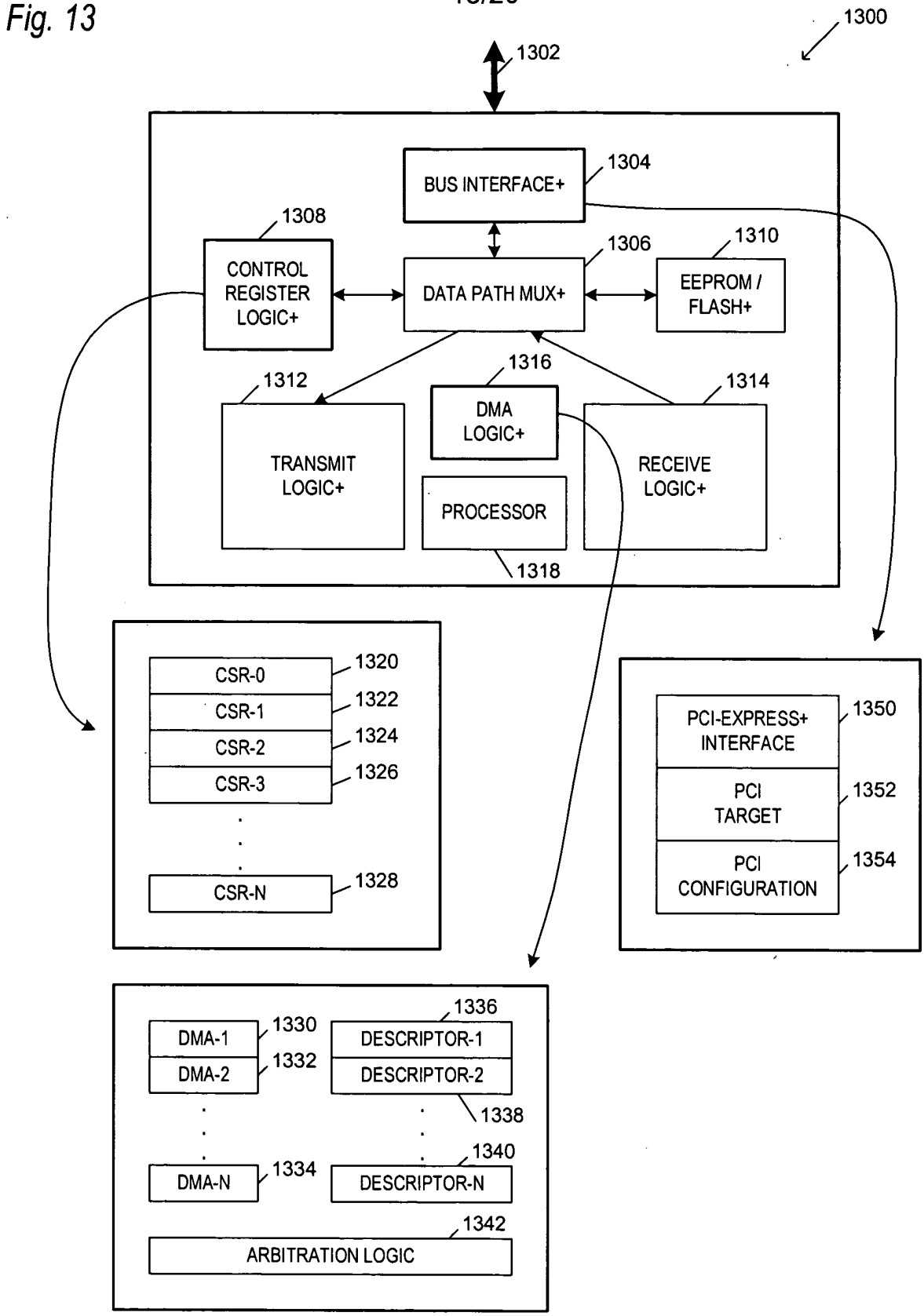

1300
1302
BUS INTERFACE+
1304
1308
CONTROL REGISTER LOGIC+
1306
DATA PATH MUX+
1310
EEPROM / FLASH+
1312
TRANSMIT LOGIC+
1316
DMA LOGIC+
1314
RECEIVE LOGIC+
PROCESSOR
1318
CSR-0
CSR-1
CSR-2
CSR-3
CSR-N
1320
1322
1324
1326
1328
PCI-EXPRESS+ INTERFACE
PCI TARGET
PCI CONFIGURATION
1350
1352
1354
DMA-1
DMA-2
DMA-N
1330
1332
1334
1336
DESCRIPTOR-1
DESCRIPTOR-2
DESCRIPTOR-N
1338
1340
1342
ARBITRATION LOGIC

Fig. 14

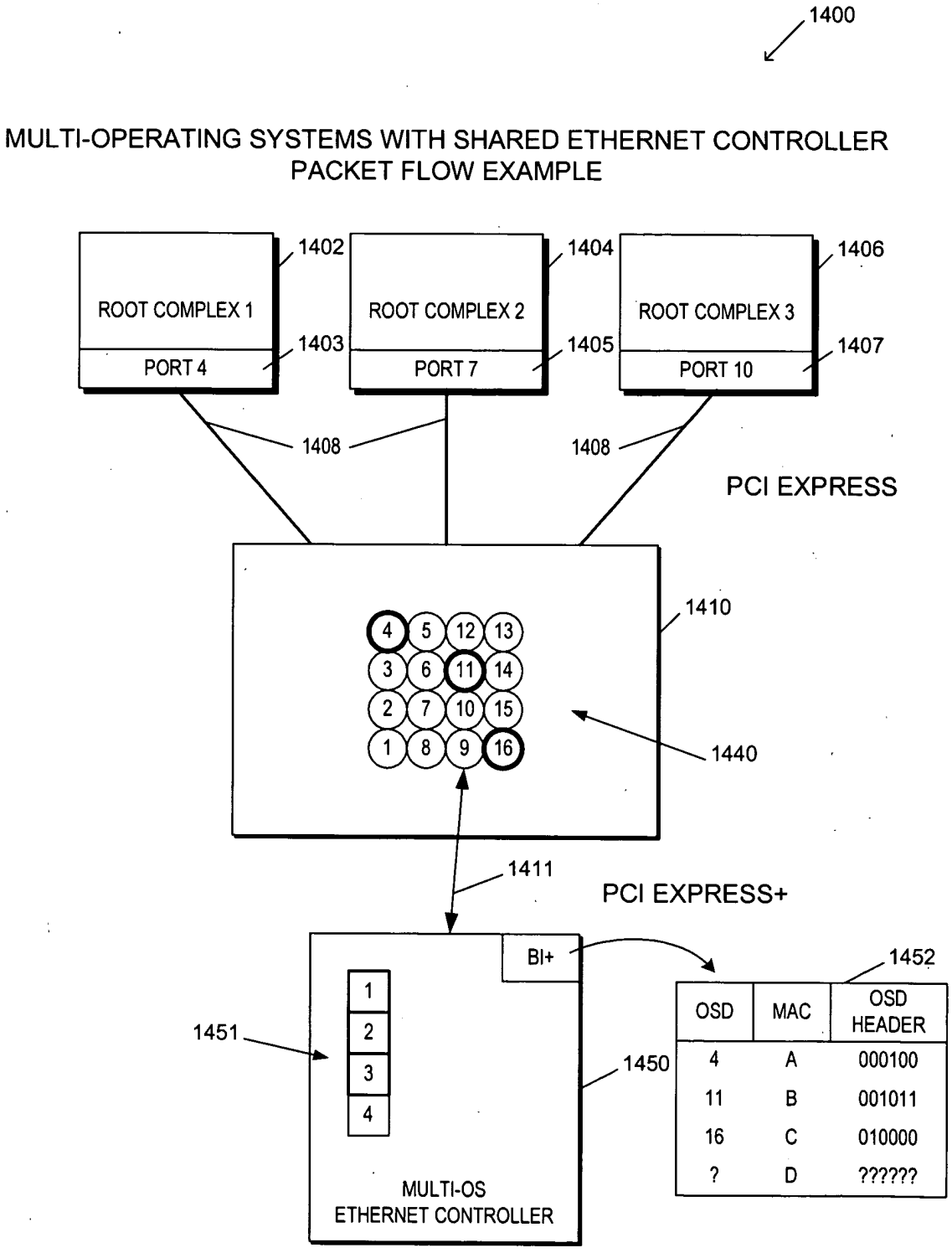

1400
MULTI-OPERATING SYSTEMS WITH SHARED ETHERNET CONTROLLER
PACKET FLOW EXAMPLE
ROOT COMPLEX 1
ROOT COMPLEX 2
ROOT COMPLEX 3
PORT 4
PORT 7
PORT 10
1402
1403
1404
1405
1406
1407
1408
1408
PCI EXPRESS
1410
4 5 12 13
3 6 11 14
2 7 10 15
1 8 9 16
1440
1411
PCI EXPRESS+
BI+
1451
1 2 3 4
1450
MULTI-OS
ETHERNET CONTROLLER
1452
OSD
MAC
OSD HEADER
4 A 000100
11 B 001011
16 C 010000
? D ??????

Fig. 15

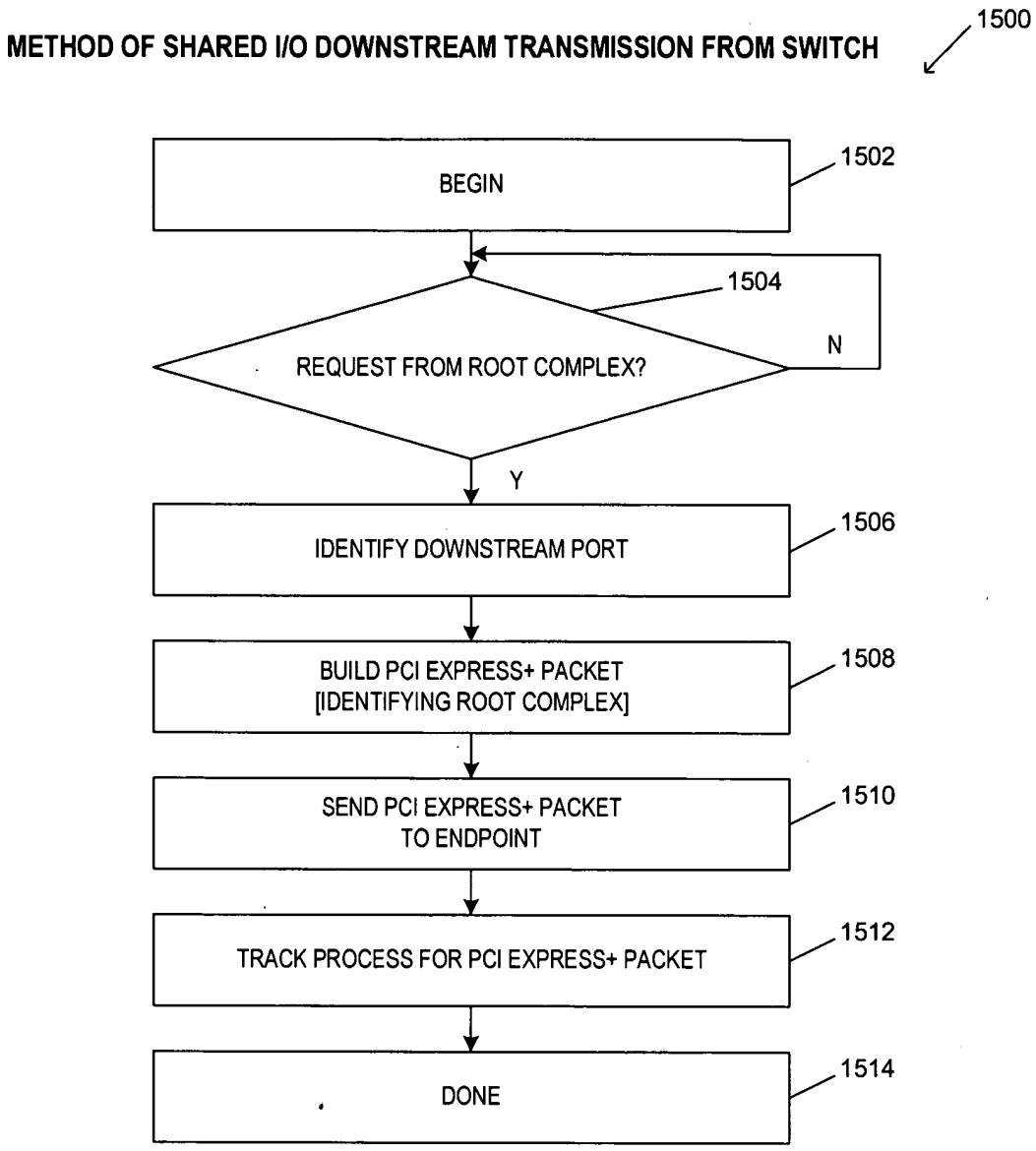

METHOD OF SHARED I/O DOWNSTREAM TRANSMISSION FROM SWITCH
1500
BEGIN
1502
1504
REQUEST FROM ROOT COMPLEX?
N
Y
IDENTIFY DOWNSTREAM PORT
1506
BUILD PCI EXPRESS+ PACKET
[IDENTIFYING ROOT COMPLEX]
1508
SEND PCI EXPRESS+ PACKET
TO ENDPOINT
1510
TRACK PROCESS FOR PCI EXPRESS+ PACKET
1512
DONE
1514

Fig. 16

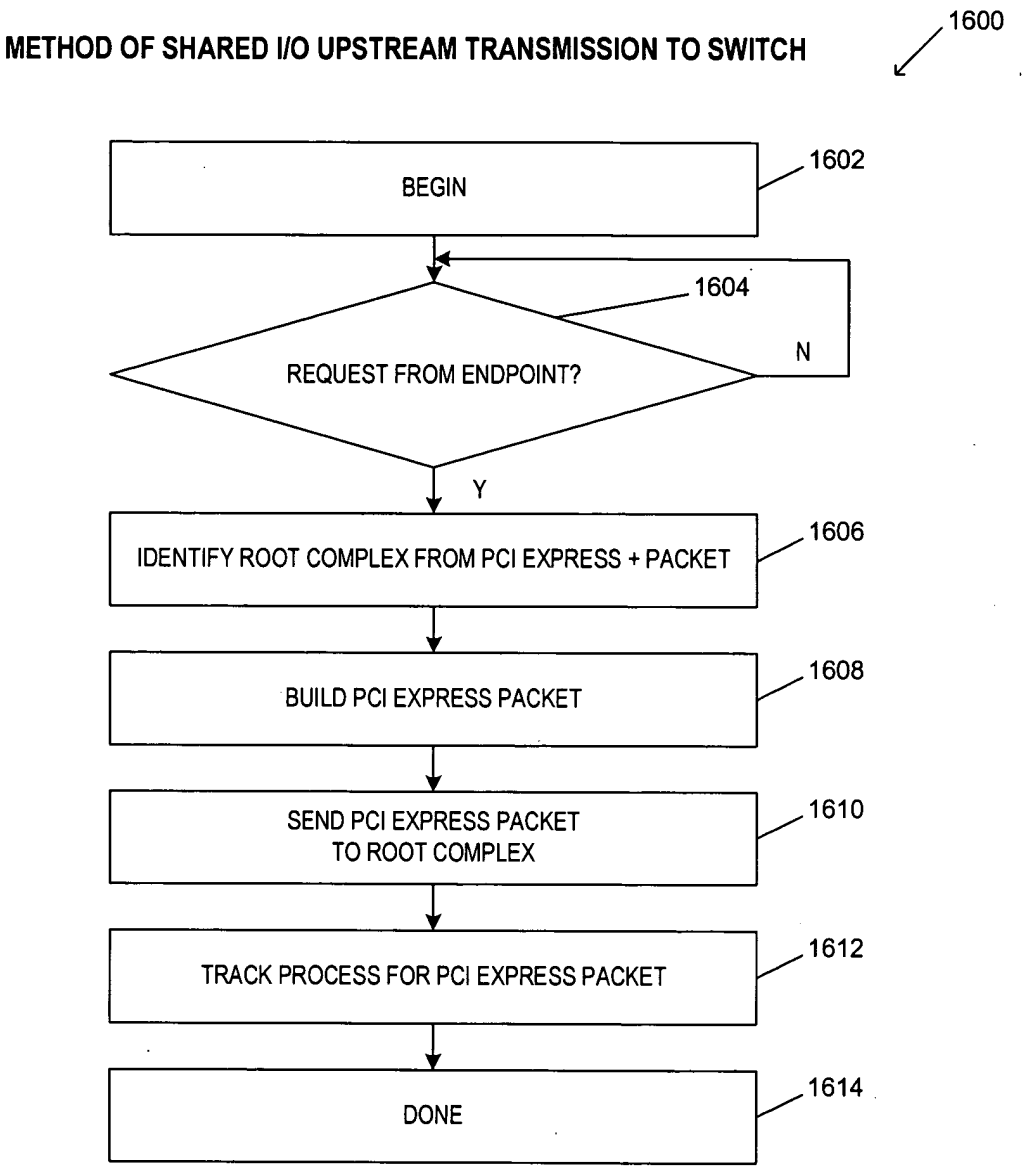

METHOD OF SHARED I/O UPSTREAM TRANSMISSION TO SWITCH
1600
BEGIN
1602
1604
REQUEST FROM ENDPOINT?
N
Y
IDENTIFY ROOT COMPLEX FROM PCI EXPRESS + PACKET
1606
BUILD PCI EXPRESS PACKET
1608
SEND PCI EXPRESS PACKET TO ROOT COMPLEX
1610
TRACK PROCESS FOR PCI EXPRESS PACKET
1612
DONE
1614

Fig. 17

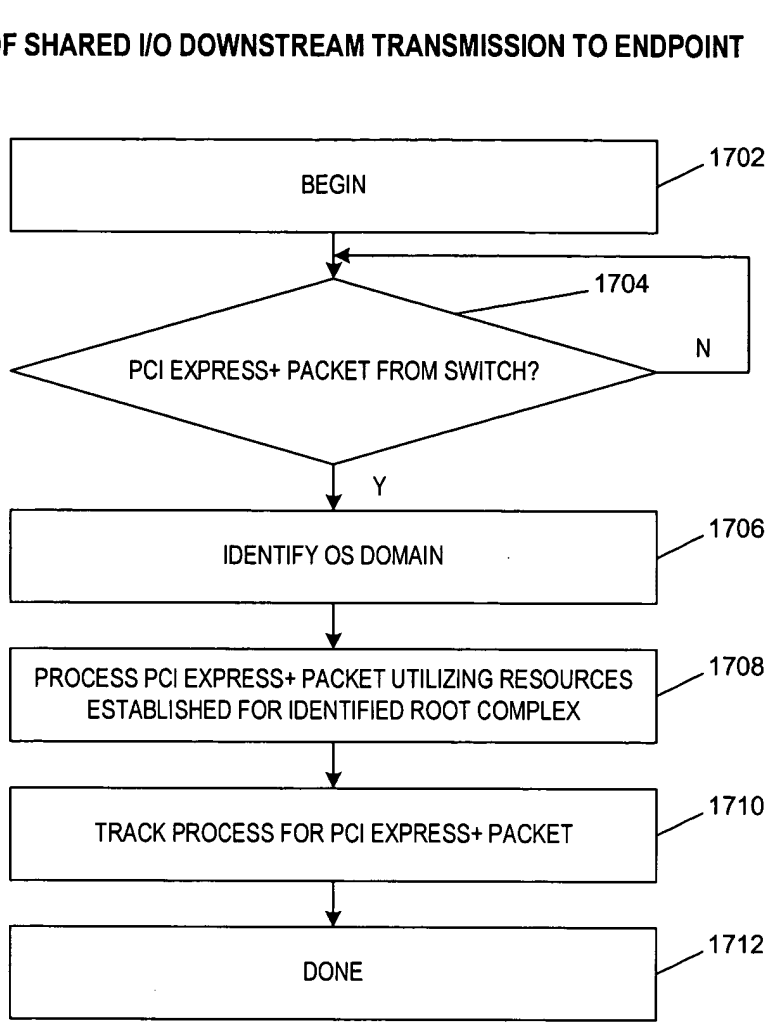

METHOD OF SHARED I/O DOWNSTREAM TRANSMISSION TO ENDPOINT
1700
BEGIN
1702
1704
PCI EXPRESS+ PACKET FROM SWITCH?
N
Y
IDENTIFY OS DOMAIN
1706
PROCESS PCI EXPRESS+ PACKET UTILIZING RESOURCES ESTABLISHED FOR IDENTIFIED ROOT COMPLEX
1708
TRACK PROCESS FOR PCI EXPRESS+ PACKET
1710
DONE
1712

Fig. 18

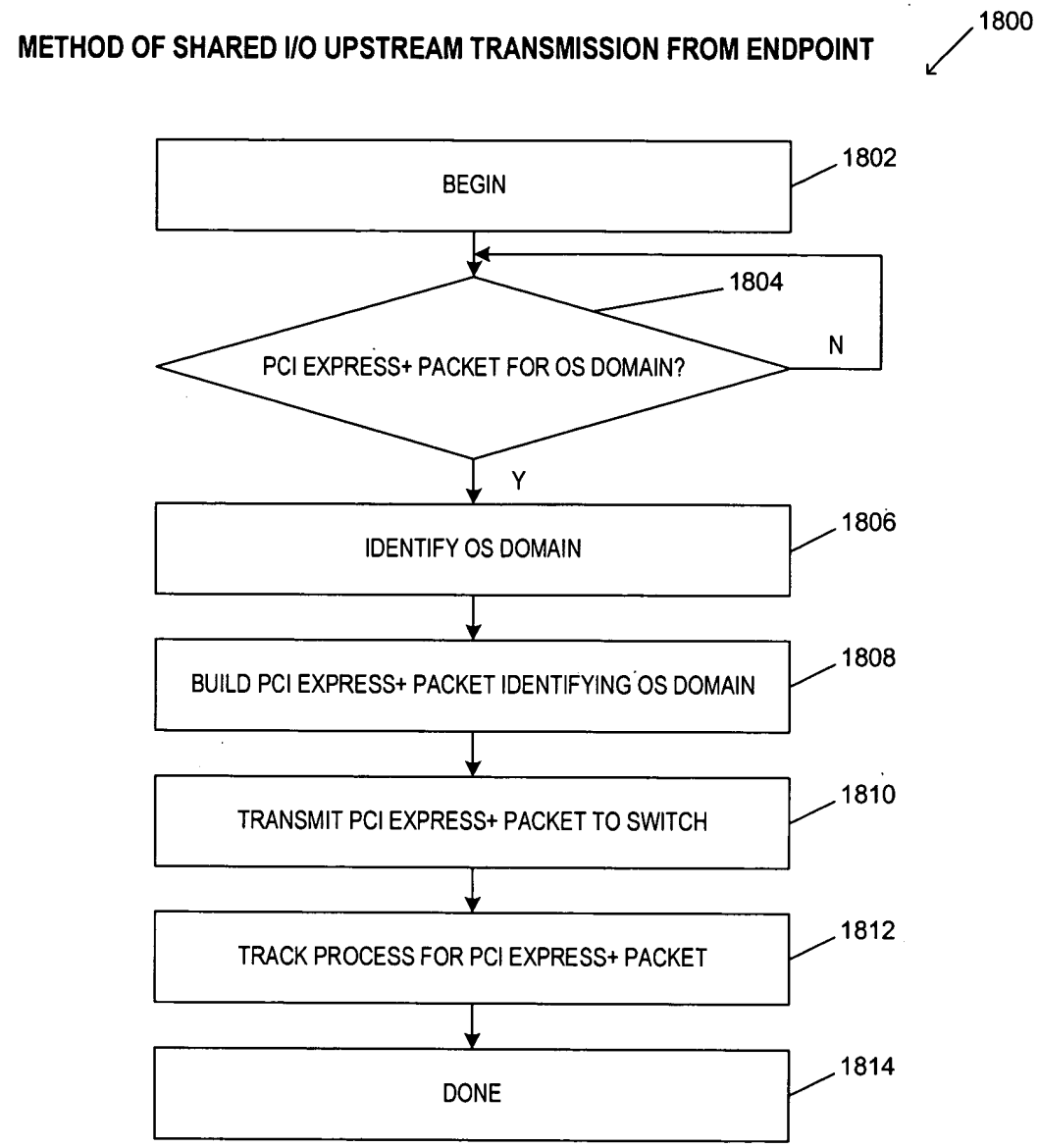

METHOD OF SHARED I/O UPSTREAM TRANSMISSION FROM ENDPOINT
1800
BEGIN
1802
1804
PCI EXPRESS+ PACKET FOR OS DOMAIN?
N
Y
IDENTIFY OS DOMAIN
1806
BUILD PCI EXPRESS+ PACKET IDENTIFYING OS DOMAIN
1808
TRANSMIT PCI EXPRESS+ PACKET TO SWITCH
1810
TRACK PROCESS FOR PCI EXPRESS+ PACKET
1812
DONE
1814

Fig. 19

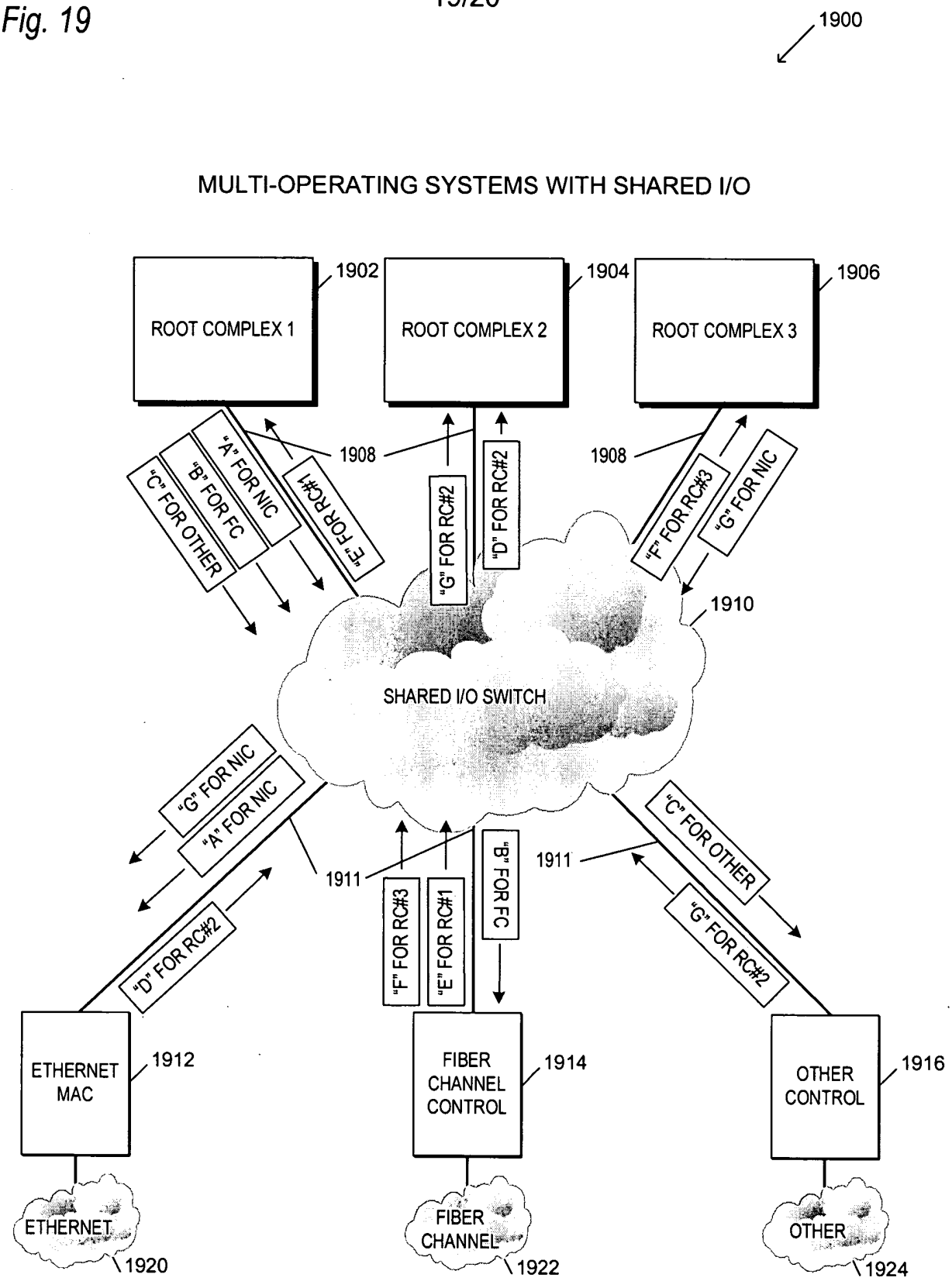
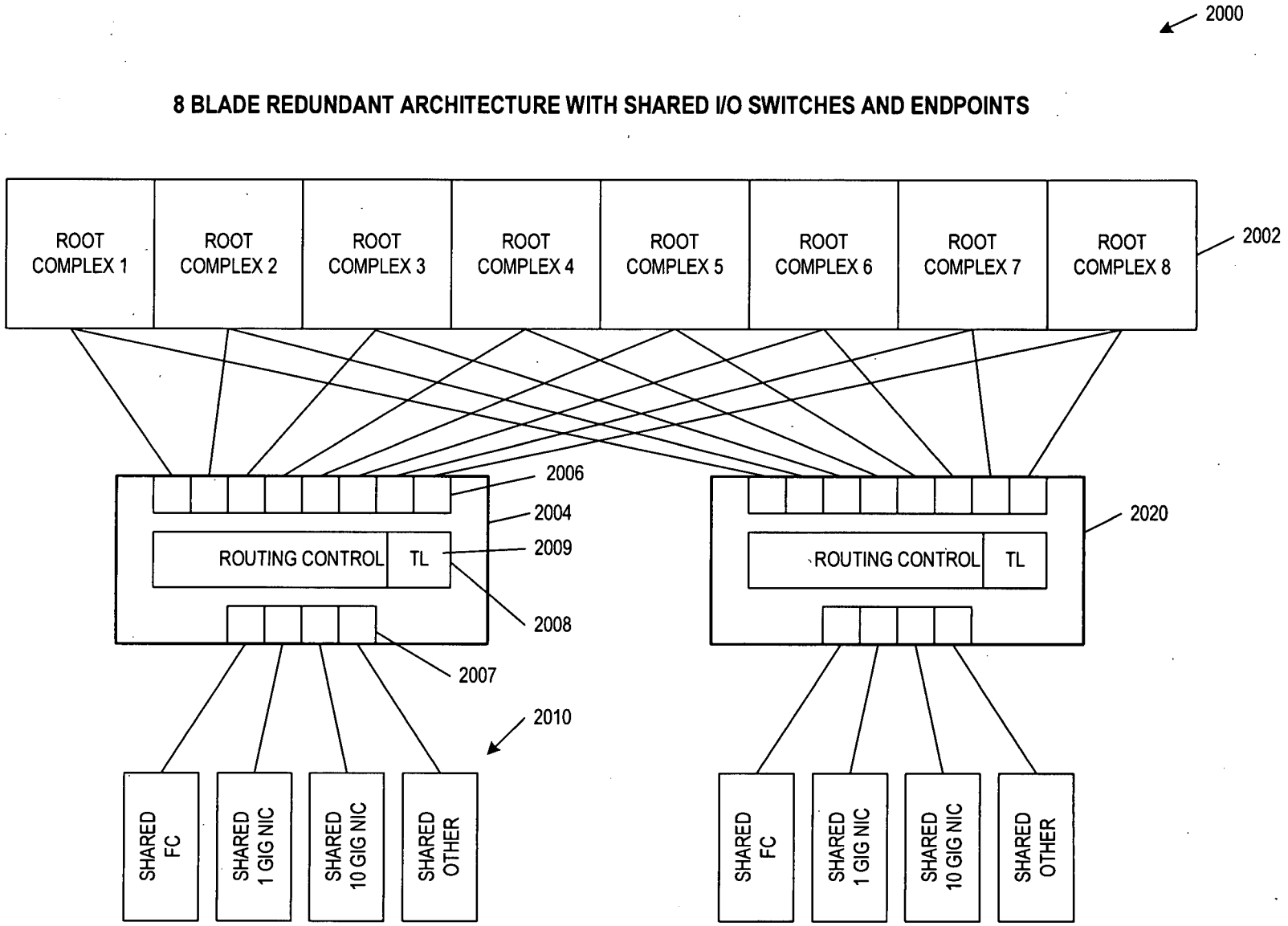

1900
MULTI-OPERATING SYSTEMS WITH SHARED I/O
ROOT COMPLEX 1
1902
ROOT COMPLEX 2
1904
ROOT COMPLEX 3
1906
1908
1908
"A" FOR NIC
"B" FOR FC
"C" FOR OTHER
"E" FOR RC#1
"G" FOR RC#2
"D" FOR RC#2
"F" FOR RC#3
"G" FOR NIC
1910
SHARED I/O SWITCH
"G" FOR NIC
"A" FOR NIC
"D" FOR RC#2
1911
1911
"F" FOR RC#3
"E" FOR RC#1
"B" FOR FC
"C" FOR OTHER
"G" FOR RC#2
ETHERNET MAC
1912
FIBER CHANNEL CONTROL
1914
OTHER CONTROL
1916
ETHERNET
1920
FIBER CHANNEL
1922
OTHER
1924

Fig. 20


2000
8 BLADE REDUNDANT ARCHITECTURE WITH SHARED I/O SWITCHES AND ENDPOINTS
ROOT COMPLEX 1
ROOT COMPLEX 2
ROOT COMPLEX 3
ROOT COMPLEX 4
ROOT COMPLEX 5
ROOT COMPLEX 6
ROOT COMPLEX 7
ROOT COMPLEX 8
2002
2006
2004
ROUTING CONTROL
TL
2009
2008
2007
2010
2020
ROUTING CONTROL
TL
SHARED FC
SHARED 1 GIG NIC
SHARED 10 GIG NIC
SHARED OTHER
SHARED FC
SHARED 1 GIG NIC
SHARED 10 GIG NIC
SHARED OTHER